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TSMC-02-513

April 30, 2004

To: Commissioner for Patents
P.O.Box 1450
Alexandria, VA 22313-1450

Fr: George O. Saile, Reg. No. 19,572
28 Davis Avenue
Poughkeepsie, N.Y. 12603

Subject: Serial No. 10/789,083 02/27/04

Bang-Ching Ho et al.

METHOD OF FORMING A DUAL DAMASCENE STRUCTURE

INFORMATION DISCLOSURE STATEMENT

Enclosed is Form PTO-1449, Information Disclosure Citation In An Application.

The following Patents and/or Publications are submitted to comply with the duty of disclosure under CFR 1.97-1.99 and 37 CFR 1.56.

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on May 4, 2004.

Stephen B. Ackerman, Reg.# 37761

Signature/Date Stephen B. Ackerman 5/4/04

U.S. Patent 6,365,529 to Hussein et al., "Method for Patterning Dual Damascene Interconnects Using a Sacrificial Light Absorbing Material," reveals a method for forming dual damascene copper interconnects using a reactive ion etching of a sacrificial layer that fills the previously formed contact hole.

U.S. Patent 6,350,681 to Chen et al., "Method of Forming Dual Damascene Structure," reveals a dual damascene process that uses a chemical mechanical polishing process to remove the barrier layer material outside the via holes.

U.S. Patent 6,268,283 to Huang, "Method for Forming Dual Damascene Structure," discloses a transparent spun on cap layer underneath the resist to prevent damage by the developer to the dielectric underlayers.

U.S. Patent 6,013,581 to Wu et al., "Method for Preventing Poisoned Vias and Trenches," discloses a dual damascene process that includes a plasma treatment of the exposed dielectric layer below the opening before the openings are filled with conductive material.

U.S. Patent 6,057,239 to Wang et al., "Dual Damascene Process Using Sacrificial Spin-On Materials," discloses a dual damascene process that exposes a portion of the oxide layer by using reactive ion etchback of the antireflective layer that filled the contact hole.

Some papers have been published that reflect on the issues of conventional dual damascene and these include using a BARC (bottom antireflective layer) layer such as in Ding et al., "Optimization of Bottom Antireflective Coating Materials for Dual Damascene Process," SPIE Proceedings, 3999,910-918(1999), Pollentier et al., "Dual Damascene back-end Patterning using 248 nm and 193 nm Lithography," Interface 2000, pps. 265-284(2000), and Gadson, Solid State Technology, pp. 77(2001).

Sincerely,

Stephen B. Ackerman,
Reg. No. 37761

Form PTO-1449

INFORMATION DISCLOSURE CITATION IN AN APPLICATION

(Use several sheets if necessary)

Docket Number (Optional)	Application Number
TSMC-02-513	10/789,083
Applicant: Bang-Ching Ho et al.	
Filing Date: 02/27/04	Group Art Unit:

U.S. PATENT DOCUMENTS

EXAMINER INITIAL	DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE
	6365529	4/2/02	Hussein et al.	438	780	2/9/00
	6350681	2/26/02	Chen et al.	438	637	2/9/01
	6268283	7/31/01	Huang	438	638	2/9/99
	6013581	1/11/00	Wu et al.	438	734	10/5/98
	6057239	5/2/00	Wang et al.	438	689	12/17/97

FOREIGN PATENT DOCUMENTS

	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	Translation YES	Translation NO

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

- Ding et al. "Optimization of Bottom Antireflective Coating Materials for Dual Damascene Process", SPIE Proceedings, 3999, (2000), pp. 910-918.
- Pollentier et al., "Dual Damascene Back-End Patterning Using 248 nm and 193 nm Lithography", Interface 2000, pp. 265-283.

EXAMINER	DATE CONSIDERED

EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP § 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to the applicant.

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—	Gadson et al., "Top Surface Imaging Improves Copper Process Resolution", Solid State Technology, pp. 1-5, 77(2001).

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